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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,195	01/20/2004	Mauro Pagliato	2110-103-3	2489

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EXAMINER	
NGUYEN, VIET Q	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/762,195	PAGLIATO ET AL.	
	Examiner	Art Unit	
	Viet Q. Nguyen	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Response filed on 9/14/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-10 and 24-26* is/are allowed.

6)☒ Claim(s) *11-14,16-19,22,23,27,28 and 30* is/are rejected.

7)☒ Claim(s) *15, 20, 21, 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/20/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In view of applicant's response, the last restriction requirement is now withdrawn, and all claims **1-30** are present for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims **11, 16, 17, 19, 22, 23, 27, 28, 30** are rejected under 35 U.S.C. 102(a) as being anticipated by **Lin et al (6,549,613).**

Lin et al (see Fig. 1) teaches a parallel sense amplifier that includes an input branch with input cell current (Icell) generated from the memory cell (20) and at least a first output branch coupled to the input branch (by a current duplicating or mirror circuit) so to generate a first reference current (I'cell) and/or a first output signal (Id1) that is r4elated to a combination of the first mirror current related to said input current. For example, Fig. 2 further shows in detail a plurality of comparators (25, 26, 27) coupled to the input cell current (Icell) and plurality of respective output current branches (Id1). However, such output current signals (Id1) is generated or related from a combination of

a first reference current (Iref1) and a first output current (Icell, right side 21) that is also related (or mirrored) to the input memory cell current (Icell, left side 21). As an example, the current comparator (25) is able to generate an output value (O1) indicating the value of input cell current (Icell) or cell voltage (Vcell) from the combination of both input current (Icell) and reference current (Iref) at the combined current compare node (211(a)).

Regarding claims 19 & 30, Lin et al also teaches the use of plurality of mirror currents and reference currents generated for one same "multi-valued" storage cell and the use of other comparators (26, 27) for generating second or third output mirrored currents (Icell) as well as second or third reference currents (Iref2, Iref3), that are also related to the cell input current (Icell) form cell transistor (2), see Fig. 2. Furthermore, these additional comparators (26, 27) are used to decode additional cell current/voltage values in response to the additional combination of additional output currents (Icell) and additional reference currents (Iref2, iref3) as claimed.

4. Claims **11-14, 16-18, 22-23, 27-28** are rejected under 35 U.S.C. 102(e) as being anticipated by **Fujita et al (6,567,330).**

Fujita et al (see Fig. 2A) teaches a sense amplifier that includes an input branch with input cell current (Icell generated from the memory cell (20) and at least a first output branch (SN) coupled to the input branch (by a current duplicating or mirror circuit 4a) so to generate a first output signal (Id1) that is also r4elated to a combination of the first reference current (Iref) and the first mirror current (2Icell) that is related to

said input current through the circuits (5) . For example, Fig. 2A further shows in detail of a voltage comparator (4b) coupled to the input mirror current (2Icell, SN) and a respective reference current branch (RSN) in order to generate the out signal (OUT). However, such output current signals (Id1) is generated by comparing the difference from a combination of a first reference current (Iref) and a first output current (2Icell) that is also related (or mirrored) to the input memory cell current (Icell) as similarly recited.

It is noted that the output signal of the comparator (400) can indicate a first state or second signal which depends on the difference of input current signal (Ic1) and the reference current signal (Iref) as well-known to one skilled in this art, thus able to determine the various stored states of a particular memory cell as well.. Furthermore, it is also noted that the comparator 94b) can compare input voltages and generate the output voltage (OUT) to determine the cell storage value onto the bit line (DQ) as claimed.

5. Claims **11, 13, 16-18, 22, 27-28** are rejected under 35 U.S.C. 102(b) as being anticipated by **Cernea et al (6,044,019).**

Cernea et al (see Fig. 12) teaches a sense amplifier that includes an input branch with input cell current (Ic, generated from the memory cell (100) and at least a first current output branch (Ic1) coupled to the input branch (by a current duplicating or mirror circuit 304) so to generate a first output signal (S) that is also r4elated to a combination of the first reference current (IR1) and said first mirror current (Ic1) that is related to said input current through the mirror circuits (304) . For example, Fig. 12

further shows in detail of a voltage comparator (400) directly coupled to the input mirror current (Ic1) and a respective reference current branch (IR1) in order to generate the out signal (S) through the encoder unit (340). However, such output current signals (S) is generated by encoding the output results of the comparator (400) after comparing the difference from a combination of a first reference current (Iref) and a first output current (Ic1) that is also related (or mirrored) to the input memory cell current (Icell) as similarly recited.

It is noted that the output signal of the comparator (400) can indicate a first state or second signal which depends on the difference of input current signal (Ic1) and the reference current signal (Iref) as well-known to one skilled in this art, thus able to determine the various stored states of a particular memory cell as well..

6. Other claims contain allowable subject matter over the prior arts of record for the following stated reasons:

- Claims **1-10** recite a parallel sense amplifier structure which uses a "multiple" current mirror and plurality of mirrored reference current branches, that are not fairly suggested in the arts or seen elsewhere;
- Claims **15 & 29** are objected as being dependent upon rejected base claims; whoever, they recite the "smaller' of first reference current and first mirror current value which are not disclosed elsewhere;

- Claims **20-21** are objected as being dependent upon rejected claim 11, but add the use of third output branch for signal comparison which is not also taught elsewhere;
- Claims **24-26** recite the specific transistor connection with comparator nodes that are not seen elsewhere;

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Viet Q. Nguyen whose telephone number is (571) 272-1788. The examiner can normally be reached on 7am-6pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dave Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

V. Nguyen
09/29/2005

VIET Q. NGUYEN
PRIMARY EXAMINER